Amendments to the Claims:

Please amend claims 1, 12, and 18, and add new claims 21 and 22, as follows:

Claim 1 (currently amended):   A method for verifying optimization of processor link for a system comprising a Northbridge, a bus coupled between a CPU and the Northbridge, and a Southbridge, the method comprising the following steps:

setting an initial bus width and an initial bus frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus width and the initial bus frequency;

generating a read request to read the Southbridge;

outputting ~~of~~ a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receives the read request, initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level;

outputting ~~of~~ a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value; ~~and~~

transforming the voltage level of the optimization verification signal to a second voltage level <u>according to the bus connection signal</u>; and

reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal <u>with the logic level transformed to the second voltage level</u>, wherein the bus operates thereafter at another bus operating bus width and another bus operating frequency.

Claim 2 (original):   The method for verifying optimization of processor link as claimed in claim 1, wherein the bus is a lightning data transport bus.

Claim 3 (original):   The method for verifying optimization of processor link as claimed in claim 1, wherein the bus is a hyper-transport bus.

Claim 4 (original):   The method for verifying optimization of processor link as claimed in claim 1, further comprising the step of setting an optimized bus operating bus width and an optimized bus operating frequency of the bus.

Claim 5 (original):   The method for verifying optimization of processor link as claimed in claim 4, wherein the bus operates at the optimized bus operating bus width and the optimized bus operating frequency when the CPU and the Northbridge are reconnected.

Claim 6 (previously presented): The method for verifying optimization of processor link as claimed in claim 1, wherein the bus disconnection signal and the bus connection signal are output by a single output terminal of the Southbridge.

Claim 7 (original):   The method for verifying optimization of processor link as claimed in claim 1, wherein the bus disconnection signal and the bus connection signal are generated by asserting and de-asserting a signal output by the Southbridge.

Claim 8 (original):   The method for verifying optimization of processor link as claimed in claim 1, wherein the optimization verification signal is output by a signal level detection circuit.

Claim 9 (original):   The method for verifying optimization of processor link as claimed in claim 8, wherein the signal level detection circuit comprises a flip-flop and an OR logic gate coupled to the flip-flop, the flip-flop outputs the optimization verification signal with the first voltage level when the Southbridge outputs the bus disconnection signal, and outputs the optimization verification signal with the second voltage level when the Southbridge outputs the bus connection signal.

Claim 10 (original):   The method for verifying optimization of processor link as claimed in claim 8, wherein the signal level detection circuit is coupled to the output terminal of the Southbridge.

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Claim 11 (original): The method for verifying optimization of processor link as claimed in claim 8, wherein the signal level detection circuit is coupled to the input terminals of the CPU or the Northbridge.

Claim 12 (currently amended): A method for verifying optimization of processor link for a system comprising a Northbridge, a bus coupled between the CPU and the Northbridge, and a Southbridge, the method comprising the following steps:

setting an initial bus width, an initial bus frequency, a bus operating bus width and a bus operating frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus width and the initial bus frequency;

setting an optimized bus operating bus width and an optimized bus operating frequency of the bus;

generating a read request to read the Southbridge;

outputting ~~of~~ a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receiving the read request, initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level;

outputting ~~of~~ a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value; ~~and~~

transforming the voltage level of the optimization verification signal to a second voltage level according to the bus connection signal; and

reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal with the logic level transformed to the second voltage level, wherein the bus operates thereafter at the optimized bus operating bus width and the optimized bus operating frequency.

Claim 13 (original): The method for verifying optimization of processor link as claimed in claim 12, wherein the bus is a lightning data transport bus.

Claim 14 (original): The method for verifying optimization of processor link as claimed in claim 12, wherein the bus is a hyper-transport bus.

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Claim 15 (previously amended):The method for verifying optimization of processor link as claimed in claim 12, wherein the bus disconnection signal and the bus connection signal are output by a single output terminal of the Southbridge.

Claim 16 (original): The method for verifying optimization of processor link as claimed in claim 12, wherein the bus disconnection signal and the bus connection signal are generated by asserting and de-asserting a signal output by the Southbridge.

Claim 17 (original): The method for verifying optimization of processor link as claimed in claim 12, wherein the optimization verification signal is output by a signal level detection circuit.

Claim 18 (currently amended): The method for verifying optimization of processor link as claimed in claim 17, wherein the signal level detection circuit comprises a flip-flop and an OR logic gate coupled to the flip-flop, the flip-flop outputs the optimization verification signal with the first voltage level when the Southbridge outputs the bus disconnection signal, and outputs the optimization verification signal with the second voltage level when the Southbridge outputs the bus connection signal signal.

Claim 19 (previously presented): The method for verifying optimization of processor link as claimed in claim 17, wherein the signal level detection circuit is coupled to the output terminal of the Southbridge.

Claim 20 (previously presented): The method for verifying optimization of processor link as claimed in claim 17, wherein the signal level detection circuit is coupled to the input terminals of the CPU or the Northbridge.

Claim 21 (new): The method for verifying optimization of processor link as claimed in claim 9, wherein the flip-flop comprises a terminal coupled to the Southbridge.

Claim 22 (new): The method for verifying optimization of processor link as claimed in claim 18, wherein the flip-flop comprises a terminal coupled to the Southbridge.

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